Amended Claims With Mark-ups to Show Changes Made

1. (Twice Amended) A test circuit for a microcontroller unit, comprising:

an input circuit that [consists of] comprises,

a first pin receiving a first signal, and

a second pin receiving a second signal; and

a test signal generating circuit that generates a test signal in response to a logical combination of the first signal and the second signal, wherein the test signal generating circuit comprises,

a counter that is enabled and disabled based on the first signal and the second signal, wherein the counter uses the second signal as a counting signal when enabled, and

a decoder that outputs the test signal when a count value from the counter reaches a prescribed count value.

2. (Twice Amended) The circuit of claim 1, wherein the test signal generating circuit comprises[:] a logic circuit that logically processes the first signal and the second signal[; a], wherein the counter [that] is enabled and disabled based on an output signal from the logic circuit[, wherein the counter uses the second signal as a counting signal when enabled; and

a decoder that outputs the test signal when a count value from the counter reaches a prescribed count value].

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